Course : IBM Hardware Configuration and Definition (HCD) for z/OS (ES96G)

Official IBM course

Practical course - 4d - 28h00 - Ref. S96
Price : 3540 € E.T.

With this training course, you'll learn how to use the Hardware Configuration Definition (HCD) function for z/OS, plan and launch dynamic reconfiguration of your zSeries hardware environment, use z/OS HCD dialog boxes to create an input/output (I/O) configuration and dynamically modify the I/O configuration. You'll learn about IOCDS and the various reports HCD can generate. You'll learn how to use a z/OS system to put theory into practice and practice working with HCD dialog boxes.

Teaching objectives

At the end of the training, the participant will be able to:

- Describe the new zSeries processor technology
- Code new zSeries processors (z9 to z196)
- Coding FICON channels and FICON CTCs
- Cascade code FICON Directors
- Create an IODF working file on az processor from scratch
- Use the CHPID mapping tool to create a validated working IODF
- Use the working IODF and create a production IODF
- Make dynamic I/O changes on a real z/OS system
- Create a parmlib LOADxx member for initial program loading (IPL)
- Display configuration graphically
- Create appropriate configuration reports
- Code coupling (CF) systems and CF links

Intended audience

Responsible for the I/O configuration contained in input/output data files (IODFs) and input/output configuration data sets (IOCDs) during their z/OS installation.

PARTICIPANTS

Responsible for the I/O configuration contained in input/output data files (IODFs) and input/output configuration data sets (IOCDs) during their z/OS installation.

PREREQUISITES

Basic knowledge of z/OS and I/O configuration.

TRAINER QUALIFICATIONS

The experts who lead the training courses are specialists in the subjects covered. They are approved by the publisher and certified for the course. They have also been validated by our teaching teams in terms of both professional knowledge and teaching skills for each course they teach. They have at least three to ten years of experience in their field and hold or have held positions of responsibility in companies.

ASSESSMENT TERMS

Assessment of targeted skills prior to training.
Assessment by the participant, at the end of the training course, of the skills acquired during the training course.
Validation by the trainer of the participant's learning outcomes, specifying the tools used: multiple-choice questions, role-playing exercises, etc.
At the end of each training course, ITTCERT provides participants with a course evaluation questionnaire, which is then analysed by our teaching teams. Participants also complete an official evaluation of the publisher.
An attendance sheet for each half-day of attendance is provided at the end of the training course, along with a certificate of completion if the participant has attended the entire session.

Prerequisites

Basic knowledge of z/OS and I/O configuration.

Practical details

Teaching methods

Training in French. Official course material in digital format and in English. Good understanding of written English.

Course schedule

1 **Official program**

- Introduction to HCD.
- Introduction to IOCP and MVSCP macros.
- HDC dialogue.
- LPAR and logic control unit concepts.
- OSA, OSA/ICC and HiperSockets.
- zSeries hardware overview.
- zSeries I/O architecture: logical channel subsystems
- Advanced DASD concepts: EAV/PAV and multiple subchannel assemblies
- FICON, FICON CTC and FICON Directors
- HCD implementation and migration.
- IPL and LOADxx member.
- Dynamic I/O reconfiguration.
- z196 HCD and use of CMT.
- CTC FICON for sysplex.
- HDC and Parallel Sysplex.

2 **Official practical work**

- Introducing your z/OS system.
- Getting to grips with the HDC.
- Codage d'un zSeries 2817.
- Ajout de directeurs FICON à votre configuration
- Incremental migration from the IOCP deck.
- Creation of a LOADxx member.
- Perform dynamic I/O.
- Coding a 2817 using CMT.
- FICON sysplex CTC coding.

Dates and locations

REMOTE CLASS
2026 : 30 June, 3 Nov.

PARIS LA DÉFENSE
2026 : 30 June, 3 Nov.