Course : VHDL, design for FPGA targets

Practical course - 4d - 28h00 - Ref. VHD
Price : 2990 CHF E.T.

★★★★☆   **4,2 / 5**

This course will enable you to acquire general skills in the use of VHDL, a language designed to represent the behavior and architecture of a digital electronic system. You'll be able to discover this language and develop your first VHDL project.

🎯 Teaching objectives

At the end of the training, the participant will be able to:

- ✓ Get to grips with the VHDL language and its many possibilities
- ✓ Know the essential syntax and constructs used in FPGA design
- ✓ Produce high-quality VHDL code that complies with FPGA synthesis constraints
- ✓ Functionally simulate a design by applying stimuli to it by writing a simple benchmark test

Intended audience
Engineers and technicians wishing to acquire general skills in the use of VHDL for FPGA design.

Prerequisites
No special knowledge required.

Practical details
Hands-on work
Use different examples to visualize VHDL concepts and develop a design flow from writing code to routing placements.

Course schedule

PARTICIPANTS
Engineers and technicians wishing to acquire general skills in the use of VHDL for FPGA design.

PREREQUISITES
No special knowledge required.

TRAINER QUALIFICATIONS
The experts leading the training are specialists in the covered subjects. They have been approved by our instructional teams for both their professional knowledge and their teaching ability, for each course they teach. They have at least five to ten years of experience in their field and hold (or have held) decision-making positions in companies.

ASSESSMENT TERMS
The trainer evaluates each participant's academic progress throughout the training using multiple choice, scenarios, hands-on work and more.
Participants also complete a placement test before and after the course to measure the skills they've developed.

1 **What is VHDL?**

- Meaning of the acronym and characteristics of VHDL.
- Language history and fields of application.
- Application fields and system description.
- Advantages/disadvantages of the language.
- Other HDL languages.
- VHDL/Verilog comparison.

2 **VHDL in the design flow**

- Circuit design steps.
- A common language: VHDL.
- Functional simulation.
- From language to circuit: synthesis.
- Multi-probe portability.
- From circuit to language: retroannotation.

3 **Hierarchy and functionality**

- Two complementary visions.
- Example of the hierarchical construction of an adder.

4 **Language basics**

- Structure of a VHDL file.
- Concurrent instructions.
- Sequential instructions.
- Memento: example of combinatorial and sequential coding.
- Sub-programs: functions and procedures.
- Common errors and test bench structure.

Hands-on work
Use of the 4-bit adder element (7-segment decoder, 1-digit BCD counter, display rotation, 4-display management).

5 **How do I describe the circuit?**

- Design unit: entity, architecture.
- The 3 levels of description (behavioral, data flow, structural).
- Combinatorial and sequential operators.
- Type conversions.
- Describe synchronous state machines.
- Describe architectures and structure circuits.

Hands-on work
Coding and simulation: 4-bit adder, 7-segment decoder, 1-digit BCD counter, display rotation, 4-display management.

6 **How do you test its operation?**

- Test bench structure.
- Unit testing and global testing.

Hands-on work
Application coding and simulation.

(7) Devaluation card test

- Presentation of the evaluation card.
- Routing placement and test on evaluation board.

Hands-on work
Evaluation card test.

(8) Language complement

- Class types (scalar and structured types, composite types).
- Attributes.